IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Hofstee, et. al.	§	Group Art Unit: 2182
	§	
	§	Examiner: Hassan, Aurangzeb
Serial No.: 10/697,903	§	
	§	Attorney Docket No.
Filed: October 30, 2003	§	AUS920030403US1
	§	
Title: System and Method for a Configurable Interface Controller	§	IBM Corporation
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/Joseph T. Van Leeuwen, Reg. No. 44,383/	June 4, 2007
Joseph T. Van Leeuwen, Reg. No. 44,383	Date

APPELLANTS' REVISED BRIEF (37 CFR § 41.37)

Sir:

A. INTRODUCTORY COMMENTS

This revised brief is filed in support of the previously filed Notice of Appeal, filed in this case on March 9, 2007, which appealed from the decision of the Examiner dated December 15, 2006 finally rejecting claims 8-27. Appellants are providing this Revised Brief in response to the Notification of Non-Compliant Appeal Brief mailed to Appellants on September 18, 2007. Applicants have provided additional explanation of subject matter defined in each independent claim as well as each means-plus-function limitation as indicated in the Notification mailed on September 18, 2007 and submits that the revised explanation complies with CFR 41.37(c)(1)(v).

The deadline for filing this Revised Appeal Brief is October 18, 2007. A one-month extension of time is believed due and is respectfully requested, payment for which is enclosed. If any further extension of time is required, the undersigned hereby authorizes the Commissioner to charge any fees for such further extension of time to Van Leeuwen & Van Leeuwen, Deposit Account No. 50-3754.

B. REAL PARTY IN INTEREST

The real party in interest in this appeal is International Business Machines Corporation, which is the assignee of the entire right, title, and interest in the above-identified patent application.

C. RELATED APPEALS AND INTERFERENCES

With respect to other prior or pending appeals, interferences, or judicial proceedings that are related to, will directly affect, be directly affected by, or have a bearing on the Board's decision in the pending appeal, there are no such prior or pending appeals, interferences, or judicial proceeding known to Appellants, Appellants' legal representative, or assignee.

D. STATUS OF CLAIMS

1. Total number of claims in application

There are 20 claims pending. Three claims are independent claims (8, 15, and 21), and the remaining claims are dependent claims.

2. Status of all claims in application

- Claims canceled: 1-7.
- Claims withdrawn from consideration but not canceled: None.
- Claims pending: 8-27.
- Claims allowed: None
- Claims rejected: 8-27.

3. Claims on appeal

The claims on appeal are: 8-27.

E. STATUS OF AMENDMENTS

All amendments have been entered in this case. No amendments have been made to the claims after the Final Office Action.

F. SUMMARY OF CLAIMED SUBJECT MATTER

Appellants provide a concise summary of the claimed subject matter as follows. Claims 8, 15, and 21 are independent claims. Note that claims 8-14 are method claims, claims 15-20 are information handling system claims, and claims 21-27 are computer program product claims. Independent claims 15 and 21 include means plus function limitations that correspond to the method steps set forth in independent claim 8. An information handling system capable of implementing Appellants' invention, as claimed in independent claim 15, is shown in Figures 43, 44A, 44B, 47A, and 47B, and 50 and described in Appellants' specification on pages 45-50, 55-59, and 64-65. Support for independent computer program product claim 21 is described in Appellants' specification on page 65, lines 25-30. In addition, support for each of the method steps and means plus function limitations of the independent claims are discussed below. The specific citations to Appellants' Figures and Specification are meant to be exemplary in nature, and do not limit the scope of the claims. In particular, the citations below do not limit the scope of equivalents as provided under 35 U.S.C. § 112, sixth paragraph.

In one aspect of Appellants' invention, claim 8 claims a method for dynamically assigning interface pins (see e.g., Figure 48, specification page 18, line 19 through page 19, line 12). These limitations are also found in the information handling system claim (claim 15) and the computer program product claim (claim 21). Support for limitations found in claims 8, 15, and 21 are as follows:

- receiving a first assignment request (Fig. 48, element 4810, specification page 60/lines 6-8, and page 59/line 17 to page 61/line 13);
- identifying one or more interface pins that correspond to the first assignment request (Fig. 48, elements 4810 and 4870, specification page 60/lines 6-8 for element 4810, page 60/lines 26-28 for element 4870, and page 59/line 17 to page 61/line 13);

- selecting a first interface controller from a plurality of interface controllers that correspond to the first assignment request (Fig. 48, element 4840, specification page 59/line 26 to page 60/line 5, and page 59/line 17 to page 61/line 13); and
- associating the identified interface pins with the selected interface controller (Fig. 48, elements 4830 and 4880, specification page 60/lines 11-17 for element 4830, page 60/line 28 to page 61/line 4 for element 4880, and page 59/line 17 to page 61/line 13).

Support for each of Appellants' means plus function limitations set forth in dependent claims is provided below. Note that general support for an information handling system and computer program product is discussed above. The specific citations to Appellant's Figures and Specification are meant to be exemplary in nature, and do not limit the scope of the claims, as provided under 35 U.S.C. § 112, sixth paragraph.

Claims 17 and 23 include the following means plus function limitations:

- means for receiving a second assignment request, the second assignment request corresponding to the identified interface pins (Fig. 48, element 4810, specification page 60/lines 6-8, and page 59/line 17 to page 61/line 13);
- means for selecting a second interface controller from the plurality of interface controllers that correspond to the second assignment request (Fig. 48, element 4860 (flex I/O B), specification page 59/line 26 to page 60/line 2, page 60/lines 17-25, page 61/lines 4-13, and page 59/line 17 to page 61/line 13); and
- means for re-associating the identified interface pins to the second interface controller (Fig. 48, elements 4850 and 4890, specification page 60/lines 17-18 for element 4850, page 61/lines 4-13 for element 4890, and page 59/line 17 to page 61/line 13).

Claims 19 and 25 include the following means plus function limitations:

- means for determining whether there are more interface pins that are not associated with the first interface controller (Fig. 48, elements 4850 and 4890, specification page 60/lines 17-18 for element 4850, page 61/lines 4-13 for element 4890, and page 59/line 17 to page 61/line 13); and
- means for assigning the non-associated interface pins to a second interface controller in response to the determination (Fig. 48, elements 4850 and 4890,

specification page 60/lines 17-18 for element 4850, page 61/lines 4-13 for element 4890, and page 59/line 17 to page 61/line 13).

Claims 20 and 26 include the following means plus function limitations:

- means for receiving data from the identified interface pins (Figs. 47A and 47B, (Device A 4740 and 4755 providing data over interface pins, specification page 56/lines 13-31, page 57/lines 1-15, and page 55/line 18 – page 59/line 17); and
- means for providing the data to the first interface controller (Figs. 47A and 47B, (Data provided to interface controller 4705, specification page 55/line 18-28, page 55/line 29 to page 56/line 13, page 56/lines 14-31, page 58/lines 5-24, page 58/line 25-page 59/line 10, page 55/line 18 – page 59/line 17, and page 64/lines 11-20).

G. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 8 – 27 stand rejected under 35 U.S.C. § 103 as allegedly being obvious, and therefore unpatentable, over U.S. Patent No. 6,366,109 to Shigeru Matsushita (hereinafter "Matsushita") in view of U.S. Patent No. 4,292,668 issued September 29, 1981 to Miller et al. (hereinafter "Miller").

H. ARGUMENTS – APPELLANTS' CLAIMS ARE NOT OBVIOUS, AND ARE THEREFORE PATENTABLE, OVER THE ART OF RECORD

Appellants' Independent Claims Are Not Obvious And Are Therefore Patentable Over Matsushita in view of Miller

Appellants submit that the Examiner has failed to establish a prima facie case of obviousness in rejecting Appellants' claim 1 over Matsushita in view of Miller. Section 2143 of the Manual of Patent Examining Procedures states as follows:

2143 Basic Requirements of a Prima Facie Case of Obviousness

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the

art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.

The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Appellants respectfully submit that the Final Office Action fails to establish a prima facie case of obviousness in rejecting Appellants' claims 8-27.

In Applicant's independent claims, Applicant claims a method, information handling system, and computer program product that each include limitations of:

- receiving a first assignment request;
- identifying one or more interface pins that correspond to the first assignment request;
- selecting a first interface controller from a plurality of interface controllers that correspond to the first assignment request; and
- associating the identified interface pins with the selected interface controller.

In contrast to the limitations claimed in each of Applicant's independent claims, Matsushita teaches a semiconductor device testing system that, among other shortcomings, simply does not teach "selecting ... [an] interface controller..." nor does Matsushita teach or suggest Applicant's claimed limitation of "associating the identified interface pins with the selected interface controller."

The Final Office Action contends that Matsushita teaches these limitations. However, as discussed below, the Office Action's reliance on Matsushita is misplaced.

Matsushita teaches "a semiconductor testing device for testing a semiconductor with a plurality of pins by applying a test signal." Figure 4 of Matsushita shows a configuration of Matsushita's pin assignment converter:

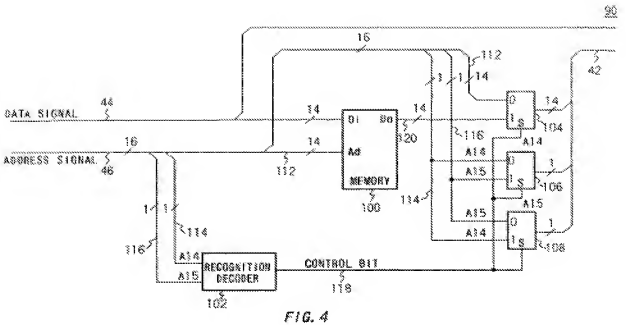

FIG. 4

The Final Office Action contends that Matsushita teaches Applicant's claimed limitation of "selecting a first interface controller from a plurality of interface controllers that correspond to the first assignment request," citing Matsushita's multiplexers (104, 106, and 108). While multiplexers are used for selecting data, the multiplexers used by Matsushita do not teach anything regarding selecting an "interface controller from a plurality of interface controllers," as claimed by Applicant. Instead, Matsushita uses the multiplexers to either replace an address signal (46) with output data (120), or leave the addresses unchanged (Matsushita, col. 6, lines 36-57). In this manner, Matsushita teaches that different semiconductor devices can be tested by replacing the pin assignment data in the pin map memory (col. 6, line 58 – col. 7, line 4).

While Matsushita may teach a system for testing semiconductor chips that are packed in different types of packages using the same test vectors and test programs (col. 6, lines 57-60), Matsushita teaches nothing regarding selecting an "interface controller from a plurality of interface controllers," as taught and claimed by Applicant. It follows that, because Matsushita is void of any teaching regarding selecting interface controllers, Matsushita is also void of any teaching regarding associating identified interface pins with a selected interface controller.

In the Final Office Action, the Examiner no longer contends that Matsushita's "recognition decoder" is analogous to Applicant's interface controller. Instead, the Final Office Action asserts that Matsushita's recognition decoder "has the functionality to proceed with the means for associating," found in Appellants' independent claims. Appellants disagree. Appellants' full limitation reads "means for associating the identified interface pins with the selected interface controller" (emphasis added). As Appellants previously discussed, Matsushita does not teach or suggest multiple interface controllers, so it follows that Matsushita does not teach or suggest "associating" any pins with a "selected interface controller." Therefore, Matsushita's "recognition decoder" is not analogous or in anyway interchangeable with Applicant's claimed "interface controller" that is selected from a plurality of interface controllers.

The Final Office Action admits that Matsushita does not teach or suggest a system having a plurality of interface controllers. The Final Office Action also admits that Matsushita does not teach or suggest Appellants' claimed limitation of "selecting a first interface controller from the plurality of interface controllers that correspond to the first assignment request." Instead, the Final Office Action attempts to combine the teachings of Matsushita with those of Miller and reasons that just because Miller teaches a plurality of interface controllers, the combination of Matsushita and Miller render Appellants' claimed invention obvious. Appellants disagree.

Neither Matsushita nor Miller teaches the limitation of selecting an interface controller

In the Final Office Action, the Examiner disagrees with this argument even though the Examiner admitted that Matsushita does not even mention an interface controller. The Examiner points out that Matsushita's multiplexers (104, 106, and 108) are no longer being cited as teaching how the interface controllers are selected. However, as pointed out above, Miller does not teach any of the selection techniques that are taught and claimed by Appellants. While Miller selects an interface controller from a plurality of controllers, Miller's selection is not based on an assignment request, where the assignment request is also used to identify interface pins.

Matsushita does not teach associating identified pins with the selected interface controller.

In the Final Office Action, the Examiner directs Applicant to figures 3 to 5 of Matsushita. However, as the Examiner already pointed out, Matsushita does not mention an interface controller. Instead, figures 3 to 5 of Matsushita are directed to a "recognition decoder" that is simply not analogous or interchangeable with Appellants' interface controller. Matsushita teaches that the "recognition decoder" is found within pin assignment converter (90) and that the recognition decoder is used to activate a control bit that is fed to a group of multiplexers in the pin assignment converter when performing semiconductor testing (see, Fig. 4 of Matsushita and col. 6, lines 9-36). The Examiner contends that "The recognition decoder assists in the means of assigning pins (logical) with the connected I/O device (physical) via interface controller as explained in column 5, lines 65-67 and column 6, lines 1-44." What Matsushita is teaching is a way of testing different semiconductor packages where the logical pin assignments to the semiconductor package remain fixed, while the physical pin numbers differ for each semiconductor package. While Matsushita's semiconductor tester re-routes logical pins to different physical pins, it does not select an interface controller from a plurality of interface controllers. In fact, Matsushita does not teach or suggest selecting any type of controller, instead it maps logical semiconductor pins to physical pin assignments in order to facilitate testing of different types of semiconductor packages. On the other hand, Miller teaches a plurality of interface controllers but does not teach selecting them based on an assignment request that also is used to identify the interface pins.

Other than teaching more than one interface controller, Miller does not teach or suggest any of the other claimed limitations.

In the Examiner's response to Appellants' argument in the Final Office Action, the Examiner states that Matsushita "already teaches a plurality of I/O devices however does not explicitly mention the fact … that an interface controller is present." This is a major problem with the Examiner's rejection. Most of the claim limitations are rejected as being taught by Matsushita. The primary focus of Appellants' claimed invention is to a "configurable interface controller." Appellants' title is a "System and Method for a Configurable Interface Controller," In Appellants' independent claims, interface pins are dynamically assigned by (1) receiving an assignment request, (2) identifying interface pins that correspond to the request, (3) selecting an interface controller from a plurality of interface controller that corresponds to the assignment

request, and then (4) associating the identified interface pins with the selected interface controller. However, here the Examiner freely admits that the primary reference does not even mention that an interface controller is even present.

Appellants point out that Matsushita is focused on a semiconductor testing device and, as the Examiner admits, does not teach or suggest anything about interface controllers. Miller, on the other hand, does teach multiple DMA interface controllers (older controllers that used to be used for handling slow speed data), however Miller's 1981 patent does not teach selecting the interface controller in any fashion at all similar to that taught and claimed by Appellants. Miller does not teach receiving an assignment request, Miller does not teach identifying pins that correspond to the request, or selecting an interface controller that corresponds to the assignment request.

In the cited section of Miller, Miller teaches an improvement to a "DMA IOC" (also known as a "DMA Controller"). Older systems, such as those described by the 25-year old Miller patent, often used DMA Controllers to communicate with I/O devices (such as printers, etc.). This was because I/O devices are very slow in comparison to the CPU, and older architectures would have the CPU spending large amounts of computer time sitting idle waiting for data from the I/O device. The DMA controller addressed this problem by providing a low-cost CPU that had enough logic and memory to handle such I/O tasks. Because these controllers had direct access to the memory, they are often referred to as "Direct Memory Access" (DMA) controllers. Modern computer systems are much faster and more complex than the computer system Miller described in his 1981 patent. Today's computers no longer "block" when waiting for data, unlike most computers that used DMA controllers. Here, Appellants' argument is not that Miller is over a quarter-century old, but instead that the type of controller being taught by Miller is fundamentally different and with that claimed by Appellants and is not combinable with the teachings of Matsushita.

Despite the fact that Miller is a relatively ancient piece of prior art discussing a type of controller that is not in widespread use today, nowhere does Miller teach or suggest "receiving an … assignment request," "identifying … interface pins that correspond to the … assignment request," "selecting a … controller … that corresponds to the assignment request," nor does

Miller teach or suggest "associating the identified pins with the selected interface controller." The Office Action Mailed July 5, 2006 cites Miller, col. 14, lines 4-24 as teaching "a plurality of interface controllers and a means for selecting a first interface controller from the plurality of interface controllers that correspond to the first assignment request." However, a review of this section of Miller shows that Miller simply does not teach "selecting a first interface controller from the plurality of interface controllers." This section of Miller, cited by the Examiner in the Office Action, is reproduced below:

> Main memory 1, 214-1, containing 48 K words and main memory 2, 216-1 containing 16 K words, are connected to system bus B 204. Memory save unit 222 is also connected to system bus B 204. System bus A 202 and system bus B 204 are connected to CPU 200, control panel 201 is directly connected to CPU 200. Diskette peripheral devices 1 and 2, 207-1 and 207-2, are connected to system bus A 202 via diskette controller 1, 206-1. Diskette peripheral devices 3 and 4, 221-1 and 221-2, are connected to system bus B 204 via diskette controller 220-1. Communication lines 1 and 2 are connected to system bus A 202 via communications controller 210-1. Printer peripheral device 209 is connected to system bus A via printer controller 208-1. The console peripheral device 213 is connected to system bus A 202 via console controller 212-1. It should be noted that a like numbered element in one figure refers to the same numbered element in another figure; for example, control panel 201 in FIG. 2 refers to the same element as shown as control panel 201 in FIG. 1.

Other than the system taught by Miller having more than one interface controller, it does not teach or suggest any of Appellants' other limitations set forth in each of Appellants' independent claims. The cited section reiterates the fact that Miller is a very old prior art reference that teaches a mainframe system with 48K of main memory that teaches an obsolete type of interface controller that are no longer used in modern systems and are not combinable with Matsushita nor interchangeable with the flexible interface controllers taught and claimed by Appellants.

The Final Office Action Admits that Matsushita does not teach selecting a first interface controller from the assignment request and added Miller for teaching a plurality of interface controllers, but the combination still does not render Appellants' claimed invention obvious.

The Examiner states that Matsushita teaches "a testing system in which pin assignment is utilized in a number variety (sic) of I/O devices." The Examiner admits that Matsushita does not

mention an interface controller is needed to connect the I/O devices. The Examiner attempts to equate the "semiconductors" that are being tested by Matsushita's device with I/O devices that would be connected to the interface controller taught and claimed by Appellants. Matsushita does not mention an I/O controller because an I/O controller is simply not used or needed to connect to the semiconductor packages that are being tested. Instead, Matsushita teaches using a semiconductor testing device 72 that is not equivalent to or interchangeable with an interface controller. Also, Matsushita teaches a single semiconductor testing device and does not teach or suggest any method of selecting the semiconductor testing device from a plurality of testing devices, in contrast to Appellants' claimed invention that teaches and claims selecting an interface controller from a plurality of interface controllers.

The Examiner concludes (para. no. 16) by stating that "one of ordinary skill in the art would recognize that Miller's teaching of how a device is connected to a system would be utilized in Matsushita's system of connected devices." Appellants respectfully disagree. As pointed out above, Miller and Matsushita are directed at two entirely different technologies. Miller is directed at multiple interface controllers and had nothing to do with semiconductor testing. Miller does not teach or suggest selecting an interface controller by receiving an assignment request, identifying pins that correspond to the request, selecting one of the controllers that corresponds to the assignment request, or associating the identified pins with the selected interface controller. Matsushita, on the other hand, teaches a way of mapping logical pins to physical semiconductor pins in order to facilitate testing of a semiconductor package but is not concerned with interface controllers and, in fact, as pointed out by the Examiner, does not even mention interface controllers. Therefore, no motivation to combine the references plausibly exists in the references themselves. Instead, one would only be motivated to combine the references after having benefit of Appellants' disclosure. The Examiner, therefore, used impermissible hindsight in selecting the references and simply used Appellants' claims as guideposts to select the references even though the references are in dissimilar fields and have no motivation to combine with each other.

Matsushita is focused on a semiconductor testing device and, as the Examiner admits, does not teach or suggest anything about interface controllers. Miller, on the other hand, does

teach multiple DMA interface controllers (older controllers that used to be used for handling slow speed data), however Miller's 1981 patent does not teach selecting the interface controller in any fashion at all similar to that taught and claimed by Appellants. Miller does not teach receiving an assignment request, Miller does not teach identifying pins that correspond to the request, or selecting an interface controller that corresponds to the assignment request.

No Motivation to Combine the Teachings of Matsushita with Those of Miller. Instead, Impermissible Hindsight Was Used in Rejecting Appellants' Claims

The Examiner's remarks to Appellants' arguments brings forth another argument of Appellants, namely, that there is no motivation to combine the teachings of Matsushita with those of Miller. The Examiner admits that Matsushita does not even mention the use of interface controllers to control I/O devices, while Miller teaches a way of sending work to slow DMA IOCs. There is no motivation to combine the references because, as the Examiner admits, Matsushita does not mention interface controllers so there is no motivation to combine the teachings of Matsushita with those of Miller as they are directed at entirely different problems and technologies. Matsushita is focused on semiconductor testing while Miller is focused on blocks of data to a particular type of interface controller. Appellants further contend that impermissible hindsight was used in rejecting Appellants' claims in view of Matsushita and Miller. No one would select these references unless they had the benefit of Appellants' disclosure. The combination of Matsushita and Miller clearly fails to teach or suggest each limitation of Applicant's claimed invention. Instead, Matsushita teaches a system that tests semiconductor chips but does not teach anything regarding more than one interface controller or how to identify an interface controller based upon a pin assignment. Miller is a very old patent and, other than having more than one interface controller, does not teach or suggest any of Appellants' claimed limitations. As described above, the combination of Matsushita in light of Miller fails to teach or suggest at least two of Applicant's claimed limitations found in each of Applicant's independent claims. Therefore, claims 8, 15, and 21 are each allowable over Matsushita in view of Miller.

Each of the remaining claims depends, directly or indirectly, on an allowable independent claim. Therefore, each of the dependent claims are also allowable for at least the same reasons as the independent claims are allowable.

Conclusion

For the foregoing reasons, Appellants submits that claims 8-27 are allowable over Matsushita in view of Miller. Accordingly, Appellants respectfully requests that the Examiner's claim rejections be reversed and claims 8-27 be allowed.

Respectfully submitted,

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I. CLAIMS APPENDIX

1. (canceled)

2. (canceled)

3. (canceled)

4. (canceled)

5. (canceled)

6. (canceled)

7. (canceled)

8. A method for dynamically assigning interface pins, said method comprising:
receiving a first assignment request;
identifying one or more interface pins that correspond to the first assignment request;
selecting a first interface controller from a plurality of interface controllers that correspond to the first assignment request; and
associating the identified interface pins with the selected interface controller.

9. The method as described in claim 8 wherein the identified interface pins are selected from the group consisting of an input interface pin and an output interface pin.

10. The method as described in claim 8 further comprising:

receiving a second assignment request, the second assignment request corresponding to the identified interface pins;

selecting a second interface controller from the plurality of interface controllers that correspond to the second assignment request; and

re-associating the identified interface pins to the second interface controller.

11. The method as described in claim 8 wherein the associating is performed using a look-up table.

12. The method as described in claim 8 further comprising:

determining whether there are more interface pins that are not associated with the first interface controller; and

assigning the non-associated interface pins to a second interface controller in response to the determination.

13. The method as described in claim 8 further comprising:

receiving data from the identified interface pins; and

providing the data to the first interface controller.

14. The method as described in claim 8 wherein the associating is performed at system initialization.

15. An information handling system comprising:

one or more processors;

one or more interface pins;

a plurality of interface controllers;

a memory accessible by the processors;

one or more nonvolatile storage devices accessible by the processors; and

an interface pin assignment tool for assigning one or more of the interface pins to one of the interface controllers, the interface pin assignment tool including:
means for receiving a first assignment request;
means for identifying one or more of the interface pins that correspond to the first assignment request;
means for selecting a first interface controller from the plurality of interface controllers that correspond to the first assignment request; and
means for associating the identified interface pins with the selected interface controller.

16. The information handling system as described in claim 15 wherein the identified interface pins are selected from the group consisting of an input interface pin and an output interface pin.

17. The information handling system as described in claim 15 further comprising:
means for receiving a second assignment request, the second assignment request corresponding to the identified interface pins;
means for selecting a second interface controller from the plurality of interface controllers that correspond to the second assignment request; and
means for re-associating the identified interface pins to the second interface controller.

18. The information handling system as described in claim 15 wherein the associating is performed using a look-up table.

19. The information handling system as described in claim 15 further comprising:

means for determining whether there are more interface pins that are not associated with the first interface controller; and
means for assigning the non-associated interface pins to a second interface controller in response to the determination.

20. The information handling system as described in claim 15 further comprising:
means for receiving data from the identified interface pins; and
means for providing the data to the first interface controller.

21. A computer program product stored on a computer operable media for dynamically changing pin to interface controller assignment:
means for receiving a first assignment request;
means for identifying one or more interface pins that correspond to the first assignment request;
means for selecting a first interface controller from a plurality of interface controllers that correspond to the first assignment request; and
means for associating the identified interface pins with the selected interface controller.

22. The computer program product as described in claim 21 wherein the identified interface pins are selected from the group consisting of an input interface pin and an output interface pin.

23. The computer program product as described in claim 21 further comprising:

means for receiving a second assignment request, the second assignment request corresponding to the identified interface pins;
means for selecting a second interface controller from the plurality of interface controllers that correspond to the second assignment request; and
means for re-associating the identified interface pins to the second interface controller.

24. The computer program product as described in claim 21 wherein the associating is performed using a look-up table.

25. The computer program product as described in claim 21 further comprising:
means for determining whether there are more interface pins that are not associated with the first interface controller; and
means for assigning the non-associated interface pins to a second interface controller in response to the determination.

26. The computer program product as described in claim 21 further comprising:
means for receiving data from the identified interface pins; and
means for providing the data to the first interface controller.

27. The computer program product as described in claim 21 wherein the associating is performed at system initialization.

J. EVIDENCE APPENDIX

Not applicable.

K. RELATED PROCEEDINGS APPENDIX

Not applicable.